UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION

The CALIFORNIA INSTITUTE OF TECHNOLOGY,	§	
	§	
Plaintiff,	§	
	§	**Civil Action No.: 6:20-cv-1042**
v.	§	
	§	**JURY TRIAL DEMANDED**
DELL TECHNOLOGIES INC. and DELL INC.,	§	
	§	
Defendants.		

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff the California Institute of Technology ("Caltech" or "Plaintiff"), by and through its undersigned counsel, complains and alleges against Dell Technologies Inc. and Dell Inc. (collectively "Dell" or "Defendants") as follows:

NATURE OF THE ACTION

1. This is a civil action for infringement of U.S. Patent No. 7,116,710, U.S. Patent No. 7,421,032, and U.S. Patent No. 7,916,781 (collectively, "the Asserted Patents") arising under the patent laws of the United States, 35 U.S.C. §§ 1 et seq.

2. Earlier this year, a jury found that Apple Inc.'s ("Apple's") and Broadcom Limited's ("Broadcom's") Wi-Fi products infringed the Asserted Patents and awarded Caltech over $1.1 billion in damages. *Caltech v. Broadcom Limited, et al.*, No. 16-cv-3714-GW, Dkt. No. 2114 (C.D. Cal. Jan. 29, 2020). As in the case against Apple and Broadcom, Caltech seeks a reasonable royalty from Dell as compensation for its infringement of the Asserted Patents.

THE PARTIES

3. Caltech is a non-profit private university organized under the laws of the State of California, with its principal place of business at 1200 East California Boulevard, Pasadena, California 91125.

4. Caltech is a world-renowned science and engineering research and education institution, where extraordinary faculty and students seek answers to complex questions, discover new knowledge, lead innovation, and transform our future. To date, 40 Caltech alumni and faculty have won a total of 41 Nobel Prizes. The mission of Caltech is to expand human knowledge and benefit society through research integrated with education. Caltech investigates the most challenging, fundamental problems in science and technology in a singularly collegial, interdisciplinary atmosphere, while educating outstanding students to become creative members of society. Caltech's investment in research has led Caltech to have more inventions disclosed and patents granted per faculty member than any other university in the nation, and to be consistently ranked as one of the top university patent portfolios in strength and number of patents issued.

5. On information and belief, defendant Dell Technologies Inc. is a Delaware corporation with its principal place of business at One Dell Way, Round Rock, Texas 78682.

6. On information and belief, defendant Dell Inc. is a Delaware corporation with its principal place of business at One Dell Way, Round Rock, Texas 78682. Dell. Inc. has additional offices at 1404 Park Center Dr., Austin, Texas, 701 E. Parmer Lane, Bldg. PS2, Austin, Texas, 12500 Tech Ridge Road, Austin, Texas, 9715 Burnet Road, Austin, Texas, and 4309 Emma Browning Avenue, Austin, Texas.

JURISDICTION AND VENUE

7. This Court has jurisdiction over the subject matter of this action under 28 U.S.C. §§ 1331 and 1338(a).

8. This Court has personal jurisdiction over Dell pursuant to due process and/or the Texas Long Arm Statute because Dell has committed and continues to commit acts of patent infringement, including acts giving rise to this action, within the State of Texas and this District, and because Dell recruits Texas residents, directly or through an intermediary located in this state, for employment inside or outside this state. The Court's exercise of jurisdiction over Dell would not offend traditional notions of fair play and substantial justice because Dell has established minimum contacts with the forum.

9. Venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391 and 1400 because a substantial part of the events or omissions giving rise to the claims occurred in this District, and Dell has committed acts of infringement and has a regular and established place of business in this District.

10. Dell has committed acts of infringement in this District, directly and/or through intermediaries, by, among other things, making, using, offering to sell, selling, and/or importing products and/or services that infringe the Asserted Patents, as alleged herein.

11. Dell has a regular and established places of business in this District including a shared corporate office at One Dell Way, Round Rock, Texas 78682. Dell is also registered to do business in Texas.

CALTECH'S ASSERTED PATENTS

12. On October 3, 2006, the United States Patent Office issued U.S. Patent No. 7,116,710, titled "Serial Concatenation of Interleaved Convolutional Codes Forming Turbo-Like Codes" (the "'710 patent"). A true and correct copy of the '710 patent is attached hereto as Exhibit A.

13. On September 2, 2008, the United States Patent Office issued U.S. Patent No. 7,421,032, titled "Serial Concatenation of Interleaved Convolutional Codes Forming Turbo-Like Codes" (the "'032 patent"). A true and correct copy of the '032 patent is attached hereto as Exhibit B. The '032 patent is a continuation of the application that led to the '710 patent.

14. On March 29, 2011, the United States Patent Office issued U.S. Patent No. 7,916,781, titled "Serial Concatenation of Interleaved Convolutional Codes Forming Turbo-Like Codes" (the "'781 patent"). A true and correct copy of the '781 patent is attached hereto as Exhibit C. The '781 patent is a continuation of the application that led to the '032 patent, which is a continuation of the application that led to the '710 patent.

15. The Asserted Patents identify Hui Jin, Aamod Khandekar, and Robert J. McEliece as the inventors (the "Inventors").

16. Caltech is the owner of all right, title, and interest in and to each of the Asserted Patents with full and exclusive right to bring suit to enforce the Asserted Patents, including the right

to recover for past damages and/or royalties prior to the expiration of the Asserted Patents on August 18, 2020.

17. The Asserted Patents are valid and enforceable.

BACKGROUND

Caltech's IRA Code Patents

18. The Asserted Patents disclose a seminal improvement to coding systems and methods. The Asserted Patents introduce a new type of error correction codes, called "irregular repeat and accumulate codes" (or "IRA codes"). The claimed methods and apparatuses are directed to encoders and decoders. The claimed encoders generate an IRA codeword from message or information bits reordering irregularly repeated instances of those bits in a randomized but known way and performing other logical operations such as summing and accumulating bits. The claimed decoders facilitate recovery of the message or information bits from the codewords even when the codewords have been corrupted by noise such as the noise that is experienced when transmitting a codeword over a wireless communications channel. These IRA codes are at least as effective at correcting errors in transmissions as prior coding techniques, such as turbo codes, but use simpler encoding and decoding circuitry and provide other technical and practical advantages, allowing for improved transmission rates and performance. Indeed, the IRA codes disclosed in the Asserted Patents enable a transmission rate close to the theoretical limit.

19. The Asserted Patents implement these novel IRA codes using novel encoders and decoders. The claims in the Asserted Patents enable a person of ordinary skill in the art to implement IRA codes using simple circuitry, providing improved performance over prior art encoders and decoders.

20. In September 2000, the Inventors of the Asserted Patents published a paper regarding their invention, titled "Irregular Repeat-Accumulate Codes" for the Second International Conference on Turbo Codes attached hereto as Exhibit D. This paper has been widely cited by experts in the field.

21. The Inventors' patents and publications describing IRA codes have been widely recognized and cited by academics and experts in the field of digital communications for their

improvements over prior art error-correction codes. For example, a paper praising these IRA codes was published in August 2004 by Aline Roumy, Souad Guemghar, Giuseppe Caire, and Sergio Verdú in the IEEE Transactions on Information Theory. This paper, titled "Design Methods for Irregular Repeat-Accumulate Codes," and attached hereto as Exhibit E, states:

> IRA codes are, in fact, special subclasses of both irregular LDPCs and irregular turbo codes. . . . IRA codes are an appealing choice because the encoder is extremely simple, their performance is quite competitive with that of turbo codes and LDPCs, and they can be decoded with a very-low-complexity iterative decoding scheme.

This paper also notes that, four years after publication of the Inventors' September 2000 paper, the Inventors were the only ones to propose a method to design IRA codes.

IEEE 802.11 Wi-Fi Standard

22. The Institute of Electrical and Electronics Engineers ("IEEE") has developed standards for wireless communications over local area networks (also referred to as "Wi-Fi"). Wi-Fi usage is widespread in modern electronic products, including smartphones, laptops, routers, televisions, cameras, cars and other devices that have wireless connections.

23. The IEEE standard upon which Wi-Fi is based is IEEE 802.11. The 802.11 standardization process began in the 1990s and the first version of 802.11 was referred to as IEEE 802.11-1997. In the following years, subsequent versions of the 802.11 standard were adopted.

24. One of the key improvements to the 802.11n version of the standard involved a "High Throughput (HT)" mode that is implemented using specific LDPC (Low-Density Parity Check) error correction codes. The same LDPC error correction codes introduced in the 802.11n version of the standard are also implemented in the subsequent 802.11ac version (finalized by IEEE in 2013 and basis for Wi-Fi 5) and 802.11ax version (nearing finalization and basis for Wi-Fi 6) of the standard. The LDPC codes specified by the 802.11n, 802.11ac, and 802.11ax standards may be implemented using Caltech's patented IRA/LDPC encoders and decoder technology.

Caltech's Case Against Apple and Broadcom

25. In May 2016, Caltech filed a patent infringement action against Apple and Broadcom in the Central District of California involving the Asserted Patents. On January 29, 2020, a jury rendered a verdict finding that Apple's and Broadcom's Wi-Fi products infringed the

Asserted Patents and awarded Caltech over $1.1 billion in damages. *Caltech v. Broadcom et al.*, No. 16-cv-3714-GW, Dkt. No. 2114 (C.D. Cal. Jan. 29, 2020).

26. The trial followed over three years of litigation during which the Court dismissed the vast majority of Apple's and Broadcom's defenses and counter-claims. For example, the Court denied Apple's and Broadcom's motion for summary judgment seeking to invalidate Caltech's '781 Patent under 35 U.S.C. § 101, and granted Caltech's motion for summary judgment of validity of Caltech's '710 and '032 Patents under 35 U.S.C. § 101. The Court also denied Apple and Broadcom's motions for summary judgment of non-infringement.

27. In addition, Apple filed ten *inter partes* review ("IPRs") petitions with the United States Patent and Trademark Office's Patent Trial and Appeal Board ("PTAB") seeking to invalidate Caltech's patents, and the PTAB either denied institution or upheld the patentability of the claims in all ten petitions.

Dell

28. Dell manufactures, uses, imports, offers for sale, and/or sells Wi-Fi products that incorporate IRA/LDPC encoders and/or decoders Asserted Patents ("Accused Products"). The Accused Products include, but are not limited to, laptops (*e.g.*, Latitude, Vostro, Inspiron, XPS, G-Series, Rugged, Chromebook Enterprise, Education, and Alienware), desktops and all-in-ones (*e.g.*, OptiPlex, Precision, Vostro, Inspiron, and XPS), tablets and 2-in-1s (*e.g.*, XPS, Latitude, Inspiron, Rugged, Chromebook Enterprise, and Education), workstations (*e.g.*, Precision), and thin clients. Upon information and belief, the Accused Products are compliant with the 802.11n, 802.11ac, and/or 802.11ax standards and the LDPC codes defined in those standards.

COUNT I

Infringement of the '710 Patent

29. Caltech re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

30. In violation of 35 U.S.C. § 271(a), Dell has infringed the '710 patent by making, using, selling, offering for sale, and/or importing into the United States, without authority, the

Accused Products which practice each and every limitation of at least claim 20 of the '710 patent. Dell has infringed literally and/or under the doctrine of equivalents.

31. Upon information and belief, the Accused Products comply with the 802.11n, 802.11ac, and/or 802.11ax standards and the 12 LDPC error correction codes defined in those standards. In addition, upon information and belief, the Accused Products are implemented in a manner that not only complies with the 802.11n, 802.11ac, and/or 802.11ax standards, but also infringes the Asserted Patents.

32. The 12 LDPC codes were originally defined in the 802.11n version of the standard and include three 1/2 rate, three 2/3 rate, three 3/4 rate, and three 5/6 rate LDPC codes as shown in Table 20-14 of the standard below.[1]

Table 20-14—LDPC parameters

Coding rate (R)	LDPC information block length (bits)	LDPC codeword block length (bits)
1/2	972	1944
1/2	648	1296
1/2	324	648
2/3	1296	1944
2/3	864	1296
2/3	432	648
3/4	1458	1944
3/4	972	1296
3/4	486	648
5/6	1620	1944
5/6	1080	1296
5/6	540	648

[1] *See* IEEE 802.11n-2009 at §20.3.11.6.2 (emphasis added); *see also* 802.11-2012 at § 20.3.11.7.2.

33. On information and belief, the Accused Products encode information or message bits using an LDPC encoder that supports the 12 LDPC codes defined in the standards. The LDPC encoder encodes the information or message bits to generate a codeword as described in Section 20.3.11.6.3 of the 802.11n standard shown below:[2]

20.3.11.6.3 LDPC encoder

For each of the three available codeword block lengths, the LDPC encoder supports rate 1/2, rate 2/3, rate 3/4, and rate 5/6 encoding. The LDPC encoder is systematic, i.e., it encodes an information block, $c=(i_0, i_1, \ldots, i_{(k-1)})$, of size k, into a codeword, **c**, of size n, $\mathbf{c}=(i_0, i_1, \ldots i_{(k-1)}, p_0, p_1, \ldots, p_{(n-k-1)})$, by adding $n-k$ parity bits obtained so that $\mathbf{H}\times\mathbf{c}^T = \mathbf{0}$, where **H** is an $(n-k)\times n$ parity-check matrix. The selection of the codeword block length (n) is achieved via the LDPC PPDU encoding process described in 20.3.11.6.5.

34. On information and belief, the LDPC encoders in the Accused Products encode information or message bits in accordance with the 12 parity-check matrices defined in the 802.11n standard. A parity-check matrix H for each of the 12 block sizes and code rates is defined in Tables R.1 to R.3 of the 802.11n. The parity-check matrix for one of the 12 LDPC codes is shown below.[3]

Table R.1 defines the matrix prototypes of the parity-check matrices for a codeword block length n=648 bits, with a subblock size Z=27 bits.

Table R.1—Matrix prototypes for codeword block length *n*=648 bits, subblock size is *Z* = 27 bits

* * *

(c) Coding rate R = 3/4.

16	17	22	24	9	3	14	-	4	2	7	-	26	-	2	-	21	-	1	0	-	-	-	-
25	12	12	3	3	26	6	21	-	15	22	-	15	-	4	-	-	16	-	0	0	-	-	-
25	18	26	16	22	23	9	-	0	-	4	-	4	-	8	23	11	-	-	-	0	0	-	-
9	7	0	1	17	-	-	7	3	-	3	23	-	16	-	-	21	-	0	-	-	0	0	-
24	5	26	7	1	-	-	15	24	15	-	8	-	13	-	13	-	11	-	-	-	-	0	0
2	2	19	14	24	1	15	19	-	21	-	2	-	24	-	3	-	2	1	-	-	-	-	0

35. Each parity-check matrix includes a left-hand side that corresponds to information or message bits, and a right-hand side that corresponds to parity bits. In the parity-check matrix shown above, the left-hand side that corresponds to information or message bits includes columns

[2] *See* IEEE 802.11n-2009 at §20.3.11.6.3(emphasis added); *see also* IEEE 802.11-2012 at § 20.3.11.7.3.

[3] *See* IEEE 802.11n-2009 at Annex R, Table R.1; *see also* IEEE 802.11-2012 at Annex F, Table F-1.

1-18, and the right-hand side that corresponds to the parity bits includes columns 19-24. The left-hand side is structured in a way that corresponds to the use of irregular repetition, scrambling and summing in the encoding process, while the right-hand side is structured in a way that corresponds to using accumulation in the encoding process. Further, the left-hand side is structured in a way that corresponds to the use of a low-density generator matrix for performing operations of irregular repetition, scrambling and summing.

36. On information and belief, the LDPC encoders in the Accused Products are implemented in a manner that meets each and every limitation of claim 20 of the '710 patent. The LDPC encoders in the Accused Products are coders. The LDPC encoders in the Accused Products include first coders which are low-density generator matrix coders and correspond to the left-hand sides of the parity-check matrices. The first coders have an input configured to receive a stream of bits (*e.g.*, information or message bits). The first coders repeat the stream of bits irregularly and scramble the repeated bits. The irregular repetition and scrambling that occurs in the LDPC encoders in the Accused Products corresponds to the irregular repetition and scrambling depicted in the left-hand sides of the parity-check matrices.

37. On information and belief, the LDPC encoders in the Accused Products include second coders which correspond to the right-hand sides of the parity-check matrices. The second coders encode bits output from the first coder at a rate within 10% of one. The encoding of output bits at a rate within 10% of one that occurs in the LDPC encoders in the Accused Products corresponds to the accumulation depicted in the right-hand sides of the parity-check matrices.

38. Dell is not licensed or otherwise authorized to practice the claims of the '710 patent.

39. By reason of Dell's infringement, Caltech has suffered substantial damages.

40. Caltech is entitled to recover the damages sustained as a result of Dell's wrongful acts in an amount subject to proof at trial.

41. Dell's infringement of the '710 patent is exceptional and entitles Caltech to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT II

Infringement of the '032 Patent

42. Caltech re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

43. In violation of 35 U.S.C. § 271(a), Dell has infringed the '032 patent by making, using, selling, offering for sale, and/or importing into the United States, without authority, the Accused Products which practice each and every limitation of at least claim 11 of the '032 patent. Dell has infringed literally and/or under the doctrine of equivalents.

44. Upon information and belief, the Accused Products comply with the 802.11n, 802.11ac, and/or 802.11ax standards and the 12 LDPC error correction codes defined in those standards. In addition, upon information and belief, the Accused Products are implemented in a manner that not only complies with the 802.11n, 802.11ac, and/or 802.11ax standards, but also infringes the Asserted Patents.

45. The 12 LDPC codes were originally defined in the 802.11n version of the standard and include three 1/2 rate, three 2/3 rate, three 3/4 rate, and three 5/6 rate LDPC codes as shown in Table 20-14 of the standard below.[4]

[4] *See* IEEE 802.11n-2009 at §20.3.11.6.2 (emphasis added); *see also* 802.11-2012 at § 20.3.11.7.2.

Table 20-14—LDPC parameters

Coding rate (R)	LDPC information block length (bits)	LDPC codeword block length (bits)
1/2	972	1944
1/2	648	1296
1/2	324	648
2/3	1296	1944
2/3	864	1296
2/3	432	648
3/4	1458	1944
3/4	972	1296
3/4	486	648
5/6	1620	1944
5/6	1080	1296
5/6	540	648

46. On information and belief, the Accused Products encode information or message bits using an LDPC encoder that supports the 12 LDPC codes defined in the standards. The LDPC encoder encodes the information or message bits to generate a codeword as described in Section 20.3.11.6.3 of the 802.11n standard shown below:[5]

20.3.11.6.3 LDPC encoder

For each of the three available codeword block lengths, the LDPC encoder supports rate 1/2, rate 2/3, rate 3/4, and rate 5/6 encoding. The LDPC encoder is systematic, i.e., it encodes an information block, $c=(i_0, i_1, \ldots, i_{(k-1)})$, of size k, into a codeword, **c**, of size n, $\mathbf{c}=(i_0, i_1, \ldots i_{(k-1)}, p_0, p_1, \ldots, p_{(n-k-1)})$, by adding $n-k$ parity bits obtained so that $\mathbf{H}\times\mathbf{c}^T = \mathbf{0}$, where **H** is an $(n-k)\times n$ parity-check matrix. The selection of the codeword block length (n) is achieved via the LDPC PPDU encoding process described in 20.3.11.6.5.

[5] *See* IEEE 802.11n-2009 at §20.3.11.6.3(emphasis added); *see also* IEEE 802.11-2012 at § 20.3.11.7.3.

47. On information and belief, the LDPC encoders in the Accused Products encode information or message bits in accordance with the 12 parity-check matrices defined in the 802.11n standard. A parity-check matrix H for each of the 12 block sizes and code rates is defined in Tables R.1 to R.3 of the 802.11n. The parity-check matrix for one of the 12 LDPC codes is shown below.[6]

Table R.1 defines the matrix prototypes of the parity-check matrices for a codeword block length n=648 bits, with a subblock size Z=27 bits.

Table R.1—Matrix prototypes for codeword block length *n*=648 bits, subblock size is *Z* = 27 bits

* * *

(c) Coding rate R = 3/4.

16	17	22	24	9	3	14	-	4	2	7	-	26	-	2	-	21	-	1	0	-	-	-	-
25	12	12	3	3	26	6	21	-	15	22	-	15	-	4	-	-	16	-	0	0	-	-	-
25	18	26	16	22	23	9	-	0	-	4	-	4	-	8	23	11	-	-	-	0	0	-	-
9	7	0	1	17	-	-	7	3	-	3	23	-	16	-	-	21	-	0	-	-	0	0	-
24	5	26	7	1	-	-	15	24	15	-	8	-	13	-	13	-	11	-	-	-	-	0	0
2	2	19	14	24	1	15	19	-	21	-	2	-	24	-	3	-	2	1	-	-	-	-	0

48. Each parity-check matrix includes a left-hand side that corresponds to information or message bits, and a right-hand side that corresponds to parity bits. In the parity-check matrix shown above, the left-hand side that corresponds to information or message bits includes columns 1-18, and the right-hand side that corresponds to the parity bits includes columns 19-24. The left-hand side is structured in a way that corresponds to the use of irregular repetition, scrambling and summing in the encoding process, while the right-hand side is structured in a way that corresponds to using accumulation in the encoding process. Further, the left-hand side is structured in a way that corresponds to the use of a low-density generator matrix for performing operations of irregular repetition, scrambling and summing.

49. A Tanner graph can be constructed from any parity-check matrix. A unique and valuable characteristic of IRA codes is apparent in the Tanner graphs for IRA codes. For example, when constructing a Tanner graph from the 12 LDPC parity-check matrices in the 802.11 standard, message bits are repeated, different subsets of the information bits are repeated different numbers

[6] *See* IEEE 802.11n-2009 at Annex R, Table R.1; *see also* IEEE 802.11-2012 at Annex F, Table F-1.

of times, check nodes are connected to information bits in a random but known pattern, parity bits are connected to check nodes which enforce a constraint that facilitates the determination of parity bits. While this is not true for a generic LDPC code, it is true for the 12 LDPC codes in the 802.11 standard.

50. On information and belief, the LDPC encoders in the Accused Products are implemented in a manner that meets each and every limitation of claim 11 of the '032 patent. The Accused Products are devices that include LDPC encoders. The LDPC encoders receive a collection of message bits and encode the message bits to generate a collection of parity bits. The LDPC encoders in the Accused Products encode the collection of message bits in accordance with the Tanner graph depicted in claim 11. The Tanner graph depicted in claim 11 is a graph representing an IRA code as a set of parity-checks where every message bit is repeated, at least two different subsets of message bits are repeated a different number of times, and check nodes, randomly connected to the repeated message bits, enforce constraints that determine the parity bits.

51. Dell is not licensed or otherwise authorized to practice the claims of the '032 patent.

52. By reason of Dell's infringement, Caltech has suffered substantial damages.

53. Caltech is entitled to recover the damages sustained as a result of Dell's wrongful acts in an amount subject to proof at trial.

54. Dell's infringement of the '032 patent is exceptional and entitles Caltech to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT III

Infringement of the '781 Patent

55. Caltech re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

56. In violation of 35 U.S.C. § 271(a), Dell has infringed the '781 patent through its use and testing of the Dell Accused Products. Through its use and testing of the Dell Accused Products, Dell performs each and every limitation of at least claim 13 of the '781 patent. Dell has infringed literally and/or under the doctrine of equivalents..

57. Upon information and belief, the Accused Products comply with the 802.11n, 802.11ac, and/or 802.11ax standards and the 12 LDPC error correction codes defined in those standards. In addition, upon information and belief, the Accused Products are implemented in a manner that not only complies with the 802.11n, 802.11ac, and/or 802.11ax standards, but also infringes the Asserted Patents.

58. The 12 LDPC codes were originally defined in the 802.11n version of the standard and include three 1/2 rate, three 2/3 rate, three 3/4 rate, and three 5/6 rate LDPC codes as shown in Table 20-14 of the standard below.[7]

Table 20-14—LDPC parameters

Coding rate (R)	LDPC information block length (bits)	LDPC codeword block length (bits)
1/2	972	1944
1/2	648	1296
1/2	324	648
2/3	1296	1944
2/3	864	1296
2/3	432	648
3/4	1458	1944
3/4	972	1296
3/4	486	648
5/6	1620	1944
5/6	1080	1296
5/6	540	648

59. On information and belief, the Accused Products encode information or message bits using an LDPC encoder that supports the 12 LDPC codes defined in the standards. The LDPC

[7] *See* IEEE 802.11n-2009 at §20.3.11.6.2 (emphasis added); *see also* 802.11-2012 at § 20.3.11.7.2.

encoder encodes the information or message bits to generate a codeword as described in Section 20.3.11.6.3 of the 802.11n standard shown below:[8]

20.3.11.6.3 LDPC encoder

For each of the three available codeword block lengths, the LDPC encoder supports rate 1/2, rate 2/3, rate 3/4, and rate 5/6 encoding. The LDPC encoder is systematic, i.e., it encodes an information block, $c=(i_0, i_1, \ldots, i_{(k-1)})$, of size k, into a codeword, **c**, of size n, $\mathbf{c}=(i_0, i_1, \ldots i_{(k-1)}, p_0, p_1, \ldots, p_{(n-k-1)})$, by adding $n-k$ parity bits obtained so that $\mathbf{H}\times\mathbf{c}^T = \mathbf{0}$, where **H** is an $(n-k)\times n$ parity-check matrix. The selection of the codeword block length (n) is achieved via the LDPC PPDU encoding process described in 20.3.11.6.5.

60. On information and belief, the LDPC encoders in the Accused Products encode information or message bits in accordance with the 12 parity-check matrices defined in the 802.11n standard. A parity-check matrix H for each of the 12 block sizes and code rates is defined in Tables R.1 to R.3 of the 802.11n. The parity-check matrix for one of the 12 LDPC codes is shown below.[9]

Table R.1 defines the matrix prototypes of the parity-check matrices for a codeword block length n=648 bits, with a subblock size Z=27 bits.

Table R.1—Matrix prototypes for codeword block length *n*=648 bits, subblock size is *Z* = 27 bits

* * *

(c) Coding rate R = 3/4.

16	17	22	24	9	3	14	-	4	2	7	-	26	-	2	-	21	-	1	0	-	-	-	-
25	12	12	3	3	26	6	21	-	15	22	-	15	-	4	-	-	16	-	0	0	-	-	-
25	18	26	16	22	23	9	-	0	-	4	-	4	-	8	23	11	-	-	-	0	0	-	-
9	7	0	1	17	-	-	7	3	-	3	23	-	16	-	-	21	-	0	-	-	0	0	-
24	5	26	7	1	-	-	15	24	15	-	8	-	13	-	13	-	11	-	-	-	-	0	0
2	2	19	14	24	1	15	19	-	21	-	2	-	24	-	3	-	2	1	-	-	-	-	0

61. Each parity-check matrix includes a left-hand side that corresponds to information or message bits, and a right-hand side that corresponds to parity bits. In the parity-check matrix shown above, the left-hand side that corresponds to information or message bits includes columns 1-18, and the right-hand side that corresponds to the parity bits includes columns 19-24. The left-hand side is structured in a way that corresponds to the use of irregular repetition, scrambling and

[8] *See* IEEE 802.11n-2009 at §20.3.11.6.3(emphasis added); *see also* IEEE 802.11-2012 at § 20.3.11.7.3.

[9] *See* IEEE 802.11n-2009 at Annex R, Table R.1; *see also* IEEE 802.11-2012 at Annex F, Table F-1.

summing in the encoding process, while the right-hand side is structured in a way that corresponds to using accumulation in the encoding process. Further, the left-hand side is structured in a way that corresponds to the use of a low-density generator matrix for performing operations of irregular repetition, scrambling and summing.

62. On information and belief, the LDPC encoders in the Accused Products are implemented in a manner that meets each and every limitation of claim 13 of the '781 patent. The LDPC encoders perform a method of encoding a signal. The LDPC encoders receive a block of data in the signal to be encoded. The block of data includes information bits. The LDPC encoders perform an encoding operation using the information bits as an input. The encoding operation includes an accumulation of mod-2 or exclusive-OR sums of bits in subsets of the information bits. The non-null values in each row in the left-hand side of the parity-check matrices correspond to the subsets of information bits that are summed.[10] The accumulation of the sums of bits in subsets of the information bits corresponds to the accumulation operations depicted in the left-hand side of the parity-check matrices.

63. Dell is not licensed or otherwise authorized to practice the claims of the '781 patent.

64. By reason of Dell's infringement, Caltech has suffered substantial damages.

65. Caltech is entitled to recover the damages sustained as a result of Dell's wrongful acts in an amount subject to proof at trial.

66. Dell's infringement of the '781 patent is exceptional and entitles Caltech to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Plaintiff hereby demands a trial by jury as to all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff respectfully prays for the following relief:

[10] The null values are represented by "-" in the parity-check matrices. The non-null values are represented by numbers.

(a) A judgment that Defendants have infringed each and every one of the Asserted Patents;

(b) Damages adequate to compensate Caltech for Defendants' infringement of the Asserted Patents pursuant to 35 U.S.C. § 284;

(c) Prejudgment interest;

(d) Post-judgment interest;

(e) A declaration that this action is exceptional pursuant to 35 U.S.C. § 285, and an award to Caltech of its attorneys' fees, costs and expenses incurred in connection with this action; and

(f) Such other relief as the Court deems just and equitable.

DATED: November 11, 2020 Respectfully submitted,

By /s/ *J. Mark Mann*

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